Modeling Parasitics in Sub-Micron IC Designs: Extract Them Before They Cost You a Re-Spin

I. Summary

IC designers who work at the deep sub-micron level know that smaller process size means lower per-unit costs, higher performance, and lower power consumption, not an end-run on the laws of physics.

As nets get closer together, parasitic capacitance becomes a design consideration. While designers have long made estimates as to where on the chip these effects might arise between layers, they are turning their attention to lateral effects within layers as they design below .25µm, where nodes become taller, thinner and denser. The best way to manage these effects is to use a parasitic extraction (PX) tool to model them in the design; the worst way is to send a chip to fabrication and have it come back faulty due to unintended influences.

This paper explains why designers must devote more attention to such parasitic effects as capacitance and resistance as process size shrinks. It describes the shortcomings of current approaches to dealing with these effects and the characteristics of a comprehensive parasitic extraction tool. Finally, it introduces ReGal PX from Tanner EDA, a high-performance, 2D/3D tool that enables designers to model parasitic effects and address them while still in the layout phase.

Main Messages

- Parasitic effects such as capacitance and resistance are more significant to overall performance at process sizes below .25µm.
- As feature size shrinks, lateral (intralayer) parasitic capacitance grows more significant than vertical (interlayer) capacitance.
- ReGal PX is a parasitic extraction tool from Tanner EDA that helps designers identify and address these effects at all process sizes with 2D and 3D modeling.

II. The Nature of Parasitic Effects

The push to pack more transistors and functionality into integrated circuits (ICs) has driven ever-smaller process sizes. Regular bulletins with foundry data compiled by the Semiconductor Industry Association (SIA) since 2005 demonstrate dramatic year-upon-year increases in production at 120nm and 90nm feature sizes, reaffirming the trend that confronts most IC designers at their desks each day: “Make it smaller.”

Shrinking process-size exacerbates certain problems on ICs, though. Sub-micron designs comprise more devices, and the devices are smaller, leading to more congested interconnect and more difficulty in isolating wires. As wires in an IC get narrower, resistance along them increases. Foundries compensate for this by making the metal layers thicker, as depicted in the blue and grey metal layers in Figure 1.

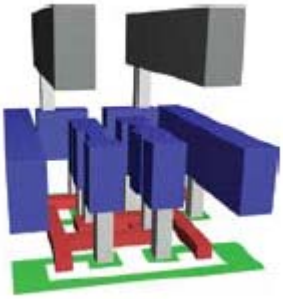

Figure 1 - SRAM Cell

With this change in the aspect ratio of the metal, interconnect coupling increases relative to device performance. Lateral capacitance can build up, as indicated by the $C_{lateral}$ term between the taller, thinner Metal 2 wires shown in Figure 2. Vertical capacitance between Metals 1 and 2 and between Metals 2 and 3 (shown as C_{vat}, C_{vft}, C_{vab} and C_{vfb}) has long figured in the calculations of IC designers, and has been easy to identify in larger-process sizes using common extraction tools, but intra-layer capacitance becomes of greater importance than inter-layer capacitance as process size shrinks below .25µm. Higher operating frequencies and lower voltages also intensify this effect.

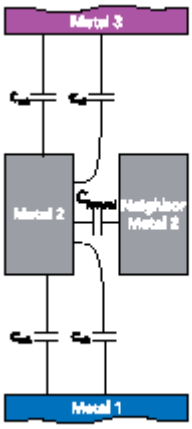

Figure 2 - Lateral Capacitance between Neighboring Metals

While some capacitance is natural and limited, lateral capacitance often brings unintended consequences in high-density chip layouts. For example, with more capacitance comes more crosstalk. A change in state in a very noisy Metal 2 node may result in an unexpected state change in a sensitive Neighbor Metal 2 node. Also, capacitance of any type loads down the node, requiring more time and power for the node to change state. Thus, the amount of parasitic capacitance on the node can have significant effects on events that are sensitive to time constants, such as signal propagation.

Designers need to allow for these consequences by including them in their simulations and accurately calculating delay and circuit behavior; otherwise, they run the risk of going through layout and tapeout to first sample back from the foundry before discovering that their chip does not work – a costly oversight.

III. Current Approaches to Extracting Parasitic Effects

To extract circuit parasitics and deliver a correct design the first time, IC designers have come up with several approaches for avoiding or identifying interconnect parasitics.

A. Prevention

Experienced designers route sensitive nodes separately from noisy nodes, keeping them far apart from one another or placing shields between them. In larger process sizes, the area of influence is relatively small, so careful prevention is often sufficient.

However, at smaller process size, it is risky to rely solely on this approach because nodes are so much closer to one another and may influence one another so much more. Also, the process of keeping noisy nodes separate from sensitive ones may be unnecessarily conservative, costing space in the design and time in the layout.

B. Extraction and simulation

Lumped capacitance to ground extraction – Several tools allow designers to extract vertical capacitance to ground from the layout, essentially a process of extracting the area and perimeter of the net and estimating a load capacitance based on that. This simple, low-cost process simulates some of the parasitic effects and results in a basic loading amount that protects against simulating faster than the circuit will actually perform; however, it does not account for shielding, crosstalk, lateral capacitance or interconnect resistance.

> How can you be certain you've correctly estimated all the parasitics when you're designing at 90nm? Do you want to bet a re-spin on it?

Informal, "back of envelope" interconnect resistance estimation – Designers may also estimate very roughly the resistance in a potentially troublesome interconnect: "It runs 500µm and is .5µm wide, so that's about *x* ohms." They manually update the netlist with the resistance, then re-run the simulation to ensure it still

works. The process is similar for roughly estimating crosstalk or any other effects not covered by extracting lumped capacitance to ground. However, the disadvantages of this time-consuming and often subjective technique are manifold, from relying on the designer's ability to anticipate all of the problem areas in the IC, to overlooking a sensitive net next to a noisy one, to underestimating the parasitic load between them, to the risk of sending an error-filled design to the foundry. It can suffice for a few, relevant parasitic interactions, but if nets are interacting in a widespread manner, then the "back of the envelope" approach becomes untenable.

At their best, then, these approaches may help extract parasitics, but at a potential cost in chip performance, silicon size and power consumption. How, then, can IC designers model interconnects and extract parasitics from a layout with maximum accuracy?

IV. Tools for Extracting Parasitics – Considerations

A well-rounded parasitic extraction tool should:

- integrate smoothly with layout, verification and simulation workflow;
- reduce the amount of guesswork and estimation in finding problematic parasitic effects;
- extract netlists of devices and parasitics, including vertical and lateral coupling capacitance and interconnect resistance;
- enable the designer to run a simulation with confidence that parasitics are accurately modeled; and
- allow the designer to optimize the mix of speed and accuracy in modeling.

A. Resistance-Capacitance (RC) extraction using finite-element interconnect network models

This technique applies a set of advanced algorithms to represent the nodes in the network as finite elements – rather than as a real-world, continuous series – each of which represents a resistor. Then, when the circuit is extracted, instead of having the transistors connected with ideal, zero-resistance lines, they will be connected through a series of resistors and capacitors comprising that network, thereby modeling the parasitic effects on each of those resistors.

B. Resistance or capacitance in isolation

The tool should also allow the designer the option of seeing either interconnect resistance or total nodal capacitance for simple extracts of one or the other in isolation. The advantage in extracting only interconnect resistance is that it helps in the identification and diagnosis of resistance-related problems that could affect the time constant of the chip, such as in the power distribution network on the chip.

V. The ReGal PX Solution from Tanner EDA

As a logical next step in its line of verification tools, Tanner has created ReGal PX, a layout-to-circuit parasitic extraction tool for sub-micron IC design. With ReGal PX, designers can model circuits in 2D or 3D, extract netlists containing interconnect parasitics, and include those netlists in simulations to calculate delay and circuit behavior accurately.

A. Implementation

ReGal PX automates the task of discovering and modeling parasitics on any cell **at frequent points during layout** rather than waiting until the end of the project, when it becomes expensive to address problems.

In **2D mode** for faster modeling, the ReGal PX engine employs a finite element method to extract interconnect

The option of 2D or 3D modeling addresses the trade-off between the accuracy of the model and the amount of time needed to generate it. 3D modeling is more accurate and better suited to small circuit blocks (<5000 transistors); 2D modeling takes less time and affords reasonably accurate interconnect models in large circuit blocks.

resistance, and an interpolation method to extract vertical and lateral coupling capacitance. In **3D mode** for greater accuracy, the engine employs an enhanced finite element method with mesh optimization to extract interconnect resistance, and a boundary element method for capacitance. Its field solver captures all relevant crosstalk, shielding, and fringing capacitance.

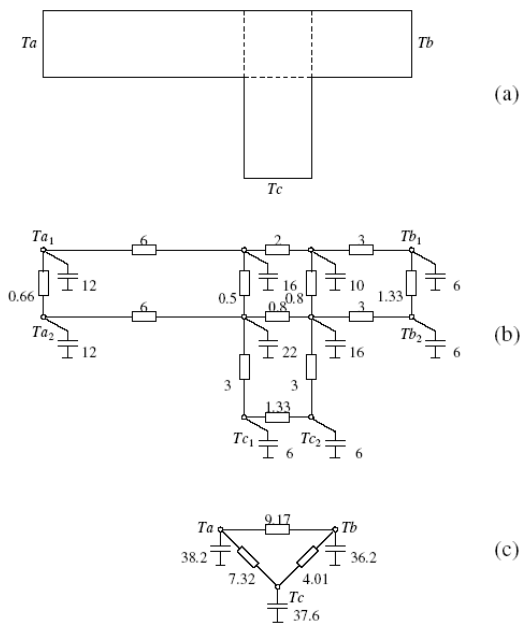

Figure 3 - Merged Resistors and Capacitors

The number of nodes in the resulting netlist – devices plus numerous resistors and capacitors due to the finite element interconnect models – can slow simulation unacceptably, so ReGal PX supports **netlist reduction.** Designers can specify the maximum frequency of interest for the circuit, and the tool will simplify the model while guaranteeing accuracy in the simulation up to that frequency. For example, Figure 3(a) depicts an original layout in a circuit and Figure 3(b) the parasitics in the circuit modeled as resistors and capacitors. When the designer applies netlist reduction and specifies a maximum frequency, ReGal PX merges resistors and capacitors throughout the circuit and models them as shown in Figure 3(c).

Specifically to model crosstalk, ReGal PX can extract vertical and lateral coupling capacitance between nets to allow **simulation of crosstalk**, rather than folding that capacitance to ground. Where crosstalk is not a concern, ReGal PX also has a mode to lump all crosstalk capacitance to ground.

ReGal PX supports hierarchical and **incremental extraction**, to model only those cells that have changed since the last extraction. In addition, designers can perform the extraction with different settings at **different hierarchy levels**, extracting smaller leaf cells, for example, in 3D mode for greater accuracy, while extracting interconnects between them in 2D mode for greater speed.

B. User interface

Tanner has integrated ReGal PX directly to its Layout Editor for smoother workflow. At any point during layout, the designer launches ReGal PX from the Layout Editor menu and sets parameters in a dialog box, as shown in Figure 4:

- Fast (2D) or Accurate (3D) modeling, depending on time constraints and the size of circuit
- Capacitance extraction, interconnect resistance extraction or both
- Circuit (netlist) reduction and maximum frequency of interest

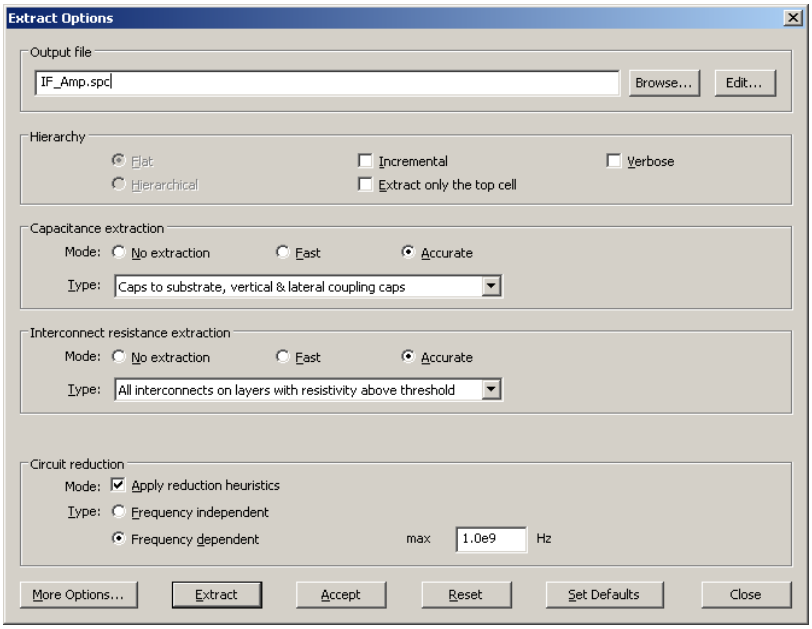

Figure 4 - Extract Options Dialog Box

C. ReGal PX workflow example

The following example design – a nine-

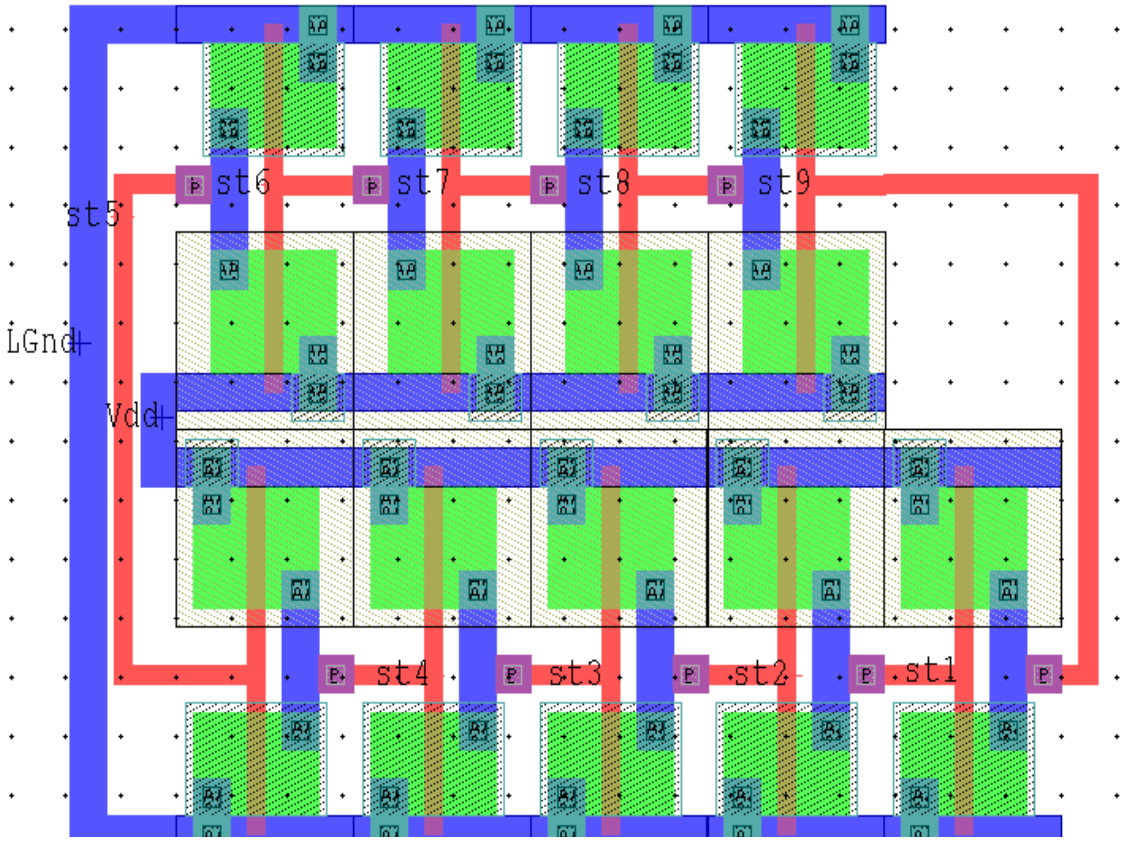

Figure 5 - Nine-Stage Ring Oscillator (Example)

stage ring oscillator shown in Figure 5 – illustrates the benefit and effectiveness of netlist reduction in ReGal PX. The design consists of 18 transistors configured into nine inverters.

When the layout is extracted without parasitics, only the 18 transistors are modeled. A SPICE simulation of this netlist yields an oscillation frequency of 1.5 GHz (upper half of Figure 6).

However, this simulation does not take interconnect parasitics into account. A second run – this time using ReGal PX 3D to extract the interconnect parasitics as a finite element RC network – results in a netlist showing the 18 transistors plus 350 parasitic resistors and capacitors.

A second simulation yields the new estimated operating frequency of 680 MHz, a difference of more than 50% (lower half of Figure 6).

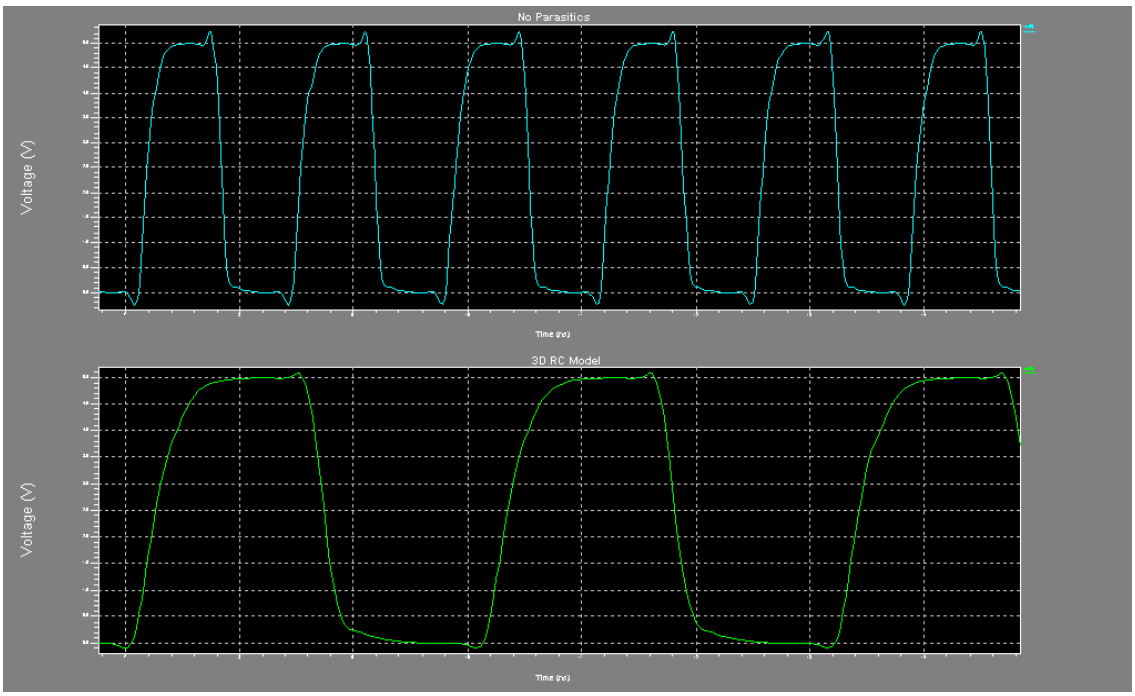

Figure 6 - Operating Frequencies Before and After Netlist Reduction

It is not surprising that the interconnect parasitics should slow down the frequency of oscillation; however, the designer may need the oscillator to run faster. Armed with the parasitic netlist, he can find the nodes most responsible and fix them. In this case, the design could extract with very simple RC models to get a compact, human-readable netlist. From that, he can see that nodes st5 and st9 in Figure 5 have excessive resistance compared to the others, due to the long routes on narrow polysilicon, and modify the design accordingly while still in Layout Editor.

VI. Conclusion

As process sizes drop below .25µm, IC designs with taller, narrower interconnects become more common. While these design techniques save space on the chip, they give way to parasitic capacitance and resistance. Designers must use software tools to model and extract these parasitic effects, or run the risk of chips that function in simulation but fail in silicon and require a re-spin.

ReGal PX from Tanner EDA optimizes parasitic extraction according to the designer's need for simulation speed and accuracy. The tool models parasitics in both 2D and 3D modes and complements existing workflow across the Tanner suite of EDA tools. ReGal PX helps designers reduce overall chip size at the sub-micron level, which translates directly to lower production costs.

VII. For More Information